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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,722	PARK, KI CHON	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 10 (line 6), "resister" should be changed to --register--; and on page 14 (lines 9-13), -- At this time, the internal clock signal (Int-CLK) generated becomes the internal clock signal (Int-CLK) for the low frequency. The internal clock signal for the low frequency has the same pulse width as those of the external clock signal but has a pulse width corresponding to the delay time of the delay signal for the external clock signal --, it is not clear what is being disclosed here.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. In claim 1, the limitation "an internal clock signal", on line 6, lacks clear antecedent basis. It is unclear if this internal clock signal is the same as the "internal clock signal" recited on line 1 of claim 1 or a different "internal clock signal". From the specification and drawings, it appears that they are the same. Furthermore, the recited limitation "the output of the operating frequency decision unit" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 2 is indefinite because of the limitation "the operating frequency decision unit generates a high frequency to determine whether the external clock signal is the high frequency or the low frequency depending on a CAS latency". It is unclear because it cannot be determined what kind of output signal of the operating frequency decision unit is being claimed here.

6. Claims 10 and 12 are indefinite because the limitations in lines 2-3 are unclear. It is not clear which preferred embodiment is referred to by those claimed limitations.

Claims 3-13 are rendered indefinite by the deficiencies of base claims 1 and 2.

7. In claim 14, the limitation "an internal clock signal", on lines 5-6, lacks clear antecedent basis. It is unclear if this internal clock signal is the same as the "internal clock signal" recited on line 1 of claim 14 or a different "internal clock signal". From the specification and drawings, it appears that they are the same signal. Furthermore, the recited limitation "the result of the determination step" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claims 15-17 are rendered indefinite by the deficiencies of base claim 14.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 5, 6, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US Pat. 5,844,438).

With regard to claims 1 and 14, Lee discloses in Figs. 2-7 a circuit, and a method of use thereof, for generating an internal clock signal, comprising an operating frequency decision unit (50) for determining whether an external clock signal (CLK) is a low frequency or a high frequency; and an internal clock signal generator (60, 70) for waveform-shaping the external clock signal and generating the internal clock signal (CLKDQ) depending on an output of the operating frequency decision unit (/OUT).

With regard to claim 5, the internal clock signal generator comprises a delay unit (61) for delaying the external clock signal by some time; and a pulse-shaping unit (62, 63) for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output of the operating frequency decision unit.

With regard to claims 6 and 13, the references also meet the recited limitations in these claims.

With regard to claim 15, in the determination step (50), whether the external clock signal (CLK) is the high frequency or the low frequency is determined as a CAS latency (/OUT).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 8, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Young (US pat. 5,028,824).

With regard to claim 8, the above discussed the circuit of Lee meets all of the claimed limitations except that the delay unit is not an RC delay circuit. Young teaches in Fig. 1 a circuit including an RC delay circuit (50). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to replace the delay unit of Lee with the RC delay circuit taught by Young in order for the resistance value of this variable resistor can be programmed (trimmed).

With regard to claim 9, the delay unit comprises a first inverter (15); the adjustable resistor (22); the adjustable capacitor (52); and a second inverter (61) connected between the first node and an output terminal. The delay unit of Lee meets all of the claimed limitations except that the adjustable resistor is not a number of resistors (R1, R2 in instant Fig. 5) serially connected; and the adjustable capacitor is not a number of MOS capacitors (C1-C3) connected to ground, as recited in the claim. However, it is notoriously well known in the art that the adjustable resistor can be configured in many different forms including a configuration as a number of resistors connected in series (see Fig. 1 of Yamato; US Pat. 6,130,571); and the adjustable capacitor can be configured in many different forms including a configuration as a number of capacitors connected in parallel (see column 15, lines 23-36 of Kono; US Pat. 6,426,671). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize those teachings with the prior art (Figs. 2-7 of Lee) for the advantage of using certain configurations which is in each case optimally matched to its application.

Claim 11 is similarly rejected, note the above discussion with regard to claim 9.

Allowable Subject Matter

12. Claims 7, 16, and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a circuit for generating an internal clock signal, as recited in claim 7, having specific structural limitation such as a pulse-shaping unit (P320 in instant Fig. 3) comprises a first NAND gate (N321) for logically combining the external clock signal (Ext_CLK) with the output signal of the delay unit (A) depending on the output (HF) of the operating frequency decision unit; a second NAND gate (N322) into which the external clock signal and the output signal of the first NAND gate are inputted; and an inverter (I321) for inverting the output signal of the second NAND gate, and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a method for generating an internal clock signal (Int_CLK in instant Fig. 3), as recited in claim 16, having specific steps such as wherein, in the determination step (as shown in Fig. 4), whether the external clock signal (Ext_CLK) is the high frequency or the low g6 frequency is determined as a CAS latency, wherein the CAS latency has a value of 0 to 7 and the external clock signal is determined as the high frequency if the value of the CAS latency is over 4, and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a method for generating an internal clock signal (Int_CLK in instant Fig. 3), as recited in claim 17, having specific steps

such as the steps of waveform-shaping (320) the external clock signal (Ext_CLK) and generating the internal clock signal if the external clock signal is the low frequency; and generating the external clock signal as the internal clock signal as it is if the external clock signal is the high frequency, and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

Conclusion

13. Regarding claims 2-4, the patentability thereof cannot be determined because of theirs indefiniteness.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
January 6, 2005

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